

**DERWENT-ACC-** 2002-452191  
**NO:**

**DERWENT-WEEK:** 200248

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**TITLE:** Method for manufacturing capacitor of semiconductor device

**INVENTOR:** YOO, Y S

**PATENT-ASSIGNEE:** HYNIX SEMICONDUCTOR INC[HYNIN]

**PRIORITY-DATA:** 2000KR-0036523 (June 29, 2000)

**PATENT-FAMILY:**

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**APPLICATION-DATA:**

<b>PUB-NO</b>	<b>APPL-DESCRIPTOR</b>	<b>APPL-NO</b>	<b>APPL-DATE</b>
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**INT-CL (IPC):** H01L021/8242

**ABSTRACTED-PUB-NO:** KR2002002082A

**BASIC-ABSTRACT:**

NOVELTY - A method for manufacturing a capacitor of a semiconductor device is provided to guarantee capacitance by using a lower electrode **seed layer using a Pt** alloy layer to easily form a lower electrode by an electroplating method, and to improve an electrical characteristic by making the lower electrode

seed layer prevent oxygen diffusion to a titanium nitride layer in forming a dielectric layer.

**DETAILED DESCRIPTION** - The first insulation layer(42) the junction part of which is opened by the first contact hole is formed on a semiconductor substrate(41). A part of the inside of the first contact hole is filled with a polysilicon layer(43). After the rest of the inside of the first contact hole is filled with a titanium silicide layer(44) and the titanium nitride layer(45), a chemical mechanical polishing process is performed. The lower electrode seed layer(46) is formed on the resultant structure. After the second insulation layer is formed on the lower electrode seed layer, the second contact hole is formed in a predetermined region of the second insulation layer. The lower electrode(48) is formed inside the second contact hole by an electroplating method. After the second insulation layer is removed, the exposed lower electrode seed layer is eliminated. The dielectric layer(49) and an upper electrode(50) are sequentially formed on the resultant structure.

**CHOSEN-DWG:** Dwg.1/10

**TITLE-TERMS:** METHOD MANUFACTURE CAPACITOR  
SEMICONDUCTOR DEVICE

**DERWENT-CLASS:** L03 U11

**CPI-CODES:** L04-C11C2; L04-C13B; L04-C14A;

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